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EXAMINER	
TRAN, MICHAEL THANH	
ART UNIT	PAPER NUMBER
2827	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/538,288	REINER, JOACHIM CHRISTIAN	
	Examiner	Art Unit	
	MICHAEL T. TRAN	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,9,10 and 16* is/are rejected.

7)☒ Claim(s) *2,4-8,11-15 and 17-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

MICHAEL TRAN
2827

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the Communications dated March 19, 2007, claims 1-20 are active in this application as a result of the addition of claims 11-20.

Drawings

2. The drawings filed June 10, 2005 have been approved.

Claim Objections

3. Claims 2, 4-8, 11-15 and 17-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 U.S.C. § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3 and 9 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Fournel et al. [U.S. Patent # 5,943,264] in view of Tsukamoto [UoS. Patent # 6,298,459].

Fournel et al. disclose, in figure 3, a one-time programmable memory device comprising an MOS (metal-oxide semiconductor) selection transistor [M1] and PN diode functioning as memory connected in series between a voltage supply line [V] and ground [Vdd], and further comprising programming means [means coupling to WL] for applying voltages to a gate of said selection transistor, to a gate of said memory transistor and to said voltage supply line, which applied voltages force said memory transistor into a snap-back mode resulting in a current thermally damaging a drain junction of said memory transistor. See Abstract and the "Summary of the Invention" sections.

Fournel et al. disclose all of the above mentioned but is silent about the fact that the memory is a MOS transistor. However, this is not new. Tsukamoto shows that it is well known that a MOS transistor connected diode is functionally equivalent to a pn diode [column 29, lines 1-6]. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Fournel et al. memory element to replace the pn diode for a MOS transistor connected diode as taught by Tsukamoto, since Tsukamoto shows that it is well known in the art that such a substitution is functionally equivalent and that it would enhance the manufacturing process of the memory device.

With respect to claim 3, both Fournel et al. and Tsukamoto disclose that the transistors are NMOS.

With respect to claim 9, Fournel et al. indicated that the memory is applicable to a CMOS technology. See Abstract and the "Background of the Invention" section.

With respect to claim 16, Fournel et al. said programming means require a setup procedure for initiating their operation, which setup procedure comprises more steps than applying one predetermined voltage level to said programming means. See the "Summary of the Invention" section.

6. Claim 10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Fournel et al. [UoS. Patent # 5,943,264] in view of Tsukamoto [U.S. Patent # 6,298,459].

Fournel et al. disclose, in figure 3, a method for programming a one-time programmable memory device comprising an MOS (metal-oxide semiconductor) selection transistor [M1] and PN diode functioning as memory connected in series between a voltage supply line [V] and ground [Vdd], and further comprising programming means [means coupling to WL] for applying voltages to a gate of said selection transistor, to a gate of said memory transistor and to said voltage supply line, which applied voltages force said memory transistor into a snap-back mode resulting in a current thermally damaging a drain junction of said memory transistor. See Abstract and the "Summary of the Invention" sections.

Fournel et al. disclose all of the above mentioned but is silent about the fact that the memory is a MOS transistor. However, this is not new. Tsukamoto shows that it is well known that a MOS transistor connected diode is functionally equivalent to a pn diode [column 29, lines 1-6]. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Fournel et al. memory element to replace the pn diode for a MOS transistor connected diode as taught by Tsukamoto, since Tsukamoto shows that it is well known in the art that such a substitution is functionally equivalent and that it would enhance the manufacturing process of the memory device.

Remarks

7. Applicant's arguments filed March 19, 2007 have been fully considered but they are not persuasive.

Applicant argued that the references, in no possible combination, could ever produce a one-time programmable memory device including the claimed features. Applicant further adds that the "Fournel reference never even disclose a memory transistor!" On the contrary, the Examiner contends that the Fournel et al. reference does, in fact, disclose the claimed "memory transistor"; and that, the combination of both references does produce a memory device with the claimed features. Applicant's attention is directed towards the Fournel et al. reference [U.S. Patent #5,943,264]. In both the Abstract and the 3rd paragraph of the "Summary of the Invention" section, Fournel et al. clearly indicated that a transistor/selection transistor series connected with

a semiconductor junction are the elements that makes up a "memory cell". Since there exists a transistor within the memory cell, it is reasonable to assume that the transistor is a "memory transistor". Therefore, the "memory transistor" of Fournel et al., in combination with the teachings of the Tsukamoto reference, would yield the claimed memory device.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for response to this final action is set to expire THREE MONTHS from the date of this action. In the event a first response is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event will the statutory period for response expire later than SIX MONTHS from the date of this final action.

Allowable Subject Matter

8. The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art of records does not show (in addition to the other elements in the claim) the following:

- Programming means comprise means for first applying a predetermined voltage to said gate of said memory transistor and for then ramping down said predetermined voltage applied to said gate of said memory transistor until said memory transistor enters said snap-back mode.
- At least one resistor-capacitor unit arranged between a voltage supply and said gate of said selection transistor and between a voltage and said gate of said memory transistor, said resistor-capacitor unit ensuring that a predetermined voltage is applied to said gate of said selection transistor and said gate of said memory transistor at the earliest a predetermined time after powering up said one-time programmable memory device. •Programming means require a setup procedure for initiating their operation, which setup procedure comprises more steps than applying one predetermined voltage level to said programming means.
- Programming means apply a programming voltage to said voltage supply line which is higher than a voltage applied to said voltage line for other operations than thermally damaging a drain junction of said memory transistor.
- readout means for applying a high voltage to said gate of said selection transistor, for applying a low voltage to said gate of said memory transistor, for applying a readout voltage to said voltage supply line, for detecting a current through said transistors resulting with said applied voltages, for comparing said detected current with a predetermined current value, and for providing an

indication that said memory transistor is programmed in case it is determined that said detected current exceeds said predetermined current value.

- a plurality of memory cells, each of said memory cells including a respective selection transistor and a respective memory transistor connected in series between said voltage supply line and ground, wherein said programming means are suited to apply voltages to said memory cells forcing any selected one of said memory transistors into a snap-back mode resulting in a current thermally damaging a drain junction of the respective memory transistor.
- applying voltages to a gate of said selection transistor, to a gate of said memory transistor and to said voltage supply line comprises first applying a predetermined voltage to said gate of said memory transistor and then ramping down said predetermined voltage applied to said gate of said memory transistor until said memory transistor enters said snap-back mode.
- at least one resistor-capacitor unit arranged between a voltage supply and said gate of said selection transistor and between a voltage supply and said gate of said memory transistor, said resistor-capacitor unit ensuring that a predetermined voltage is applied to said gate of said selection transistor and said gate of said memory transistor at the earliest a predetermined time after powering up said one-time programmable memory device.
- programming means apply a programming voltage to said voltage supply line which is higher than a voltage applied to said voltage line for other operations than thermally damaging a drain junction of said memory transistor.

Conclusion

When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-1650.

Michael T. Tran
Art Unit 2827
May 25, 2007